What is claimed is:

1. A method of fabricating a semiconductor Insulated-Gate Field-Effect Transistor (Gated-FET), comprising:

depositing a semiconductor thin film layer on an insulator; and

forming a substantially rectangular channel region in said semiconductor region, said region lightly doped to form a resistive channel region; and

depositing a gate insulator layer above said channel region; and

depositing a gate material above said insulator layer, said material forming a gate region above said channel region; and

optimizing said thin film properties, gate insulator properties and gate material properties such that said gate region further comprises:

a first voltage level that modulates said channel resistance to a substantially non-conductive state; and

a second voltage level that modulates said channel resistance to a substantially conductive state.

2. The method of claim 1, wherein said semiconductor thin film layer comprises one of a single crystal Silicon, polycrystalline Silicon, re-crystallized Silicon, Silicon on Insulator, any other semiconductor material, and any other combination of semiconductor materials.

3. The method of claim 1, wherein said insulator layer comprises one of an oxide layer, oxy-nitride layer, nitride layer, any other dielectric material, and any other combination of dielectric materials.

4. The method of claim 1, wherein said gate material comprises one of a heavily doped

thin film poly Silicon layer, salicided heavily doped poly Silicon layer, refractory metal layer and a metal layer.

5. The method of claim 1, wherein optimizing said gate material properties is further comprised of selecting a gate material comprising:

a higher work function with respect to said thin film channel region work function, when said channel region is doped with N type dopant; and

a lower work function with respect to said thin film channel region work function, when said channel region is doped with P type dopant.

6. The method of claim 1, comprising forming a source region and a drain region on opposite sides of said substantially rectangular channel region in said semiconductor thin film layer, further comprised of:

doping said source region to a higher level than said channel region, said dopant type same as said channel region; and

doping said drain region to a higher level than said channel region, said dopant type same as said channel region; and

providing a conducting path from said source region to said drain region through said resistive channel region in the middle.

7. The method of claim 1, wherein depositing said semiconductor thin film layer further comprises:

defining a surface voltage as $\Phi_S = V_D - V_{FB} - T_G * Q_S / \varepsilon_G$; and

defining a surface dopant level as $N_S = D * \exp(q\Phi_S/kT)$; and

defining a first thickness as $L_D = [\varepsilon_S * kT/(q^2 N_S)]^{0.5}$; and

defining a second thickness as $X_A = \sqrt{2}*L_D*[(N_S/D)^{0.5} - 1]$; and

defining a surface charge as $Q_S = q*N_S*X_A / (1 + X_A/(\sqrt{2}*L_D))$; and

iteratively identifying the consistent set of values that satisfies said definitions; and

depositing a substantially uniform thickness T_S of said semiconductor thin film layer, wherein said thickness T_S is greater than said second thickness X_A;

where, V_D is power supply voltage level, ε_S is channel semiconductor permittivity, ε_G is gate insulator permittivity, T_G is gate insulator thickness, V_{FB} is gate material to semiconductor channel absolute flat band voltage, k is the Boltzmann's constant, T is the absolute temperature, q is electron charge and D is channel region doping level.

8. The method of claim 1, wherein depositing said semiconductor thin film layer further comprises:

defining a first thickness as $X = \varepsilon_S*T_G/\varepsilon_G$, and

defining a second thickness as $Y = [(2*\varepsilon_S*(V_{FB} - V_T))/ (q*D)]^{0.5}$; and

defining a third thickness as $Z = (X^2+Y^2)^{0.5} - X$; and

depositing a substantially uniform thickness T_S of said semiconductor thin film layer, wherein said thickness T_S satisfies a thickness range approximately 0.8*Z to 1.2*Z;

where, ε_S is channel semiconductor permittivity, ε_G is gate insulator permittivity, T_G is gate insulator thickness, V_{FB} is gate material to semiconductor channel absolute flat band voltage, V_T is channel region absolute threshold voltage, q is electron charge and D is channel region doping level.

9. The method of claim 1, wherein said gate insulator material comprises an oxide, said gate material comprises a heavily doped poly Silicon material with opposite type dopant to said channel region, and depositing said semiconductor thin film layer further comprises:

defining a first thickness as $X = 3*T_{OX}$ (Angstroms) ; and

defining a second thickness as $Y = 0.28/\sqrt{D}$ (Angstroms) ; and

defining a third thickness as $Z = (X^2+Y^2)^{0.5} - X$ (Angstroms) ; and

depositing a substantially uniform thickness T_S of said semiconductor thin film layer, wherein said thickness T_S further satisfies a thickness range approximately 0.8*Z to 1.2*Z;

where, T_{OX} is gate oxide thickness in Angstroms, D is channel doping level in atoms/(Angstroms)^3 and T_S is channel semiconductor layer thickness in Angstroms.

10. The method of claim 1, comprised of forming one of N channel or P channel Gated-FET thin film transistor consisting a process sequence comprised of:

depositing one of amorphous or crystalline poly-1 (P1);

performing P1 mask & etching P1;

applying blanket Gated-NFET V_T N- implant;

applying Gated-PFET V_T mask & P- implant;

depositing Gox;

depositing one of amorphous or crystalline poly-2 (P2);

applying blanket P+ implantation of Gated-NFET Gate;

applying N+ mask & implanting Gated-PFET Gate;

applying P2 mask & etching P2;

applying blanket LDN N implant (Gated-NFET LDD);

applying LDP mask & P implant (Gated-PFET LDD);

depositing a spacer oxide and etching the spacer oxide;

depositing Nickel;

salicidizing the Nickel on exposed P1 and P2;

salicidizing P1 completely;

performing RTA anneal, P1 and P2 re-crystallization and dopant anneal;

depositing ILD oxide & CMP;

applying C2 mask & etch;

forming a W plug & CMP; and

depositing M1.

11. The method of claim 1, comprised of forming one of N channel or P channel thinned down SOI Gated-FET thin film transistor consisting a process sequence comprised of:

forming SOI substrate wafer;

performing Shallow Trench isolation: Trench Etch, Trench Fill and CMP;

depositing Sacrificial oxide;

applying Periphery PMOS V_T mask & implant;

applying Periphery NMOS V_T mask & implant;

applying Gated-FET mask and Silicon etch;

performing Gated-FET blanket V_T N implant;

applying Gated-FET V_T P mask and P implant;

performing Dopant activation and anneal;

performing Sacrificial oxide etch;

depositing Gate oxide / Dual gate oxide option;

depositing Gate poly (GP);

applying Gated-FET N+ mask and N+ implant;

applying Gated-FET P+ mask and P+ implant;

applying GP mask & etch;

applying LDN mask & N- implant;

applying LDP mask & P- implant;

depositing Spacer oxide & spacer etch;

applying Periphery N+ mask and N+ implant;

applying Periphery P+ mask and P+ implant;

depositing Ni;

performing RTA anneal - Ni salicidation (S/D/G regions & interconnect);

performing Dopant activation;

performing Unreacted Ni etch;

depositing ILD oxide & CMP; and

applying contact mask and etch.

12. The method of claim 6, wherein the absolute value of said channel region threshold voltage V_T comprises a value in the range from 0.18 to 0.40 times a system power voltage level.

13. A method of fabricating a semiconductor N channel Gated-FET transistor, comprising:

depositing a semiconductor thin film layer on an insulator; and

forming a substantially rectangular channel region in said semiconductor region, said region lightly doped with N type dopant to form a resistive channel region; and

forming a source region and a drain region on opposite sides of said rectangular channel region in said first semiconductor thin film layer, said source and drain regions heavily doped with N type dopant; and

depositing a gate insulator layer above said channel region; and

depositing a heavily P type doped poly-silicon gate material above said insulator layer, said gate material forming a gate region above said channel region; and

optimizing said thin film properties, gate insulator properties and gate material properties such that said gate region further comprises:

a first voltage level that modulates said channel resistance to a substantially non-conductive state, said state disconnecting said source from said drain region; and

a second voltage level that modulates said channel resistance to a substantially conductive state, said state connecting said source to said drain region.

14. The method of claim 13, wherein said first voltage level comprises a voltage in the range from system ground voltage level to a threshold voltage level, wherein:

said thin film channel is fully depleted of majority carriers; and

said source region is decoupled from said drain region for a drain to source differential bias voltage ranging from zero to a system power supply voltage.

15. The method of claim 13, wherein said second voltage level comprises a voltage in the range from said threshold voltage level to a flat band voltage level, wherein:

said thin film channel is not fully depleted, said channel comprising majority carriers; and

said source region is coupled to said drain region for a differential bias voltage ranging from zero to a system power supply voltage.

16. The method of claim 13, wherein said second voltage level comprises a voltage in the range from said flat band voltage level to a system power voltage level, wherein:

said thin film channel majority carrier concentration is substantially enhanced above said channel doping level by an accumulation near the gate insulator surface; and

said source region is coupled to said drain region for a differential bias voltage ranging from

zero to a system power supply voltage.

17. A method of fabricating a semiconductor P-channel Gated-FET transistor, comprising:

depositing a semiconductor thin film layer on an insulator; and

forming a substantially rectangular channel region in said semiconductor region, said region lightly doped with P type dopant to form a resistive channel region; and

forming a source region and a drain region on opposite sides of said rectangular channel region in said first semiconductor thin film layer, said source and drain regions heavily doped with P type dopant; and

depositing a gate insulator layer above said channel region; and

depositing a heavily N type doped poly-silicon gate material above said insulator layer, said gate material forming a gate region above said channel region; and

optimizing said thin film properties, gate insulator properties and gate material properties such that said gate region further comprises:

a first voltage level that modulates said channel resistance to a substantially non-conductive state, said state disconnecting said source from said drain region; and

a second voltage level that modulates said channel resistance to a substantially conductive state, said state connecting said source to said drain region.

18. The method of claim 17, wherein said first voltage level comprises a voltage in the range from a system power voltage level to a threshold voltage below system power voltage level, wherein:

said thin film channel is fully depleted of majority carriers; and

said source region is decoupled from said drain region for a source to drain differential bias voltage ranging from zero to said system power supply voltage.

19. The method of claim 17, wherein said second voltage level comprises a voltage in the range from a flat band voltage level below system power voltage level to said threshold voltage below system power voltage level, wherein:

said thin film channel is not fully depleted, said channel comprising majority carriers; and

said source region is coupled to said drain region for a differential bias voltage ranging from zero to said system power supply voltage.

20. The method of claim 17, wherein said second voltage level comprises a voltage range from a system ground voltage level to said flat band voltage level below system power voltage level, wherein:

said thin film channel majority carrier concentration is substantially enhanced above said channel doping level by an accumulation near the gate insulator surface; and

said source region is coupled to said drain region for a differential bias voltage ranging from zero to said system power supply voltage.